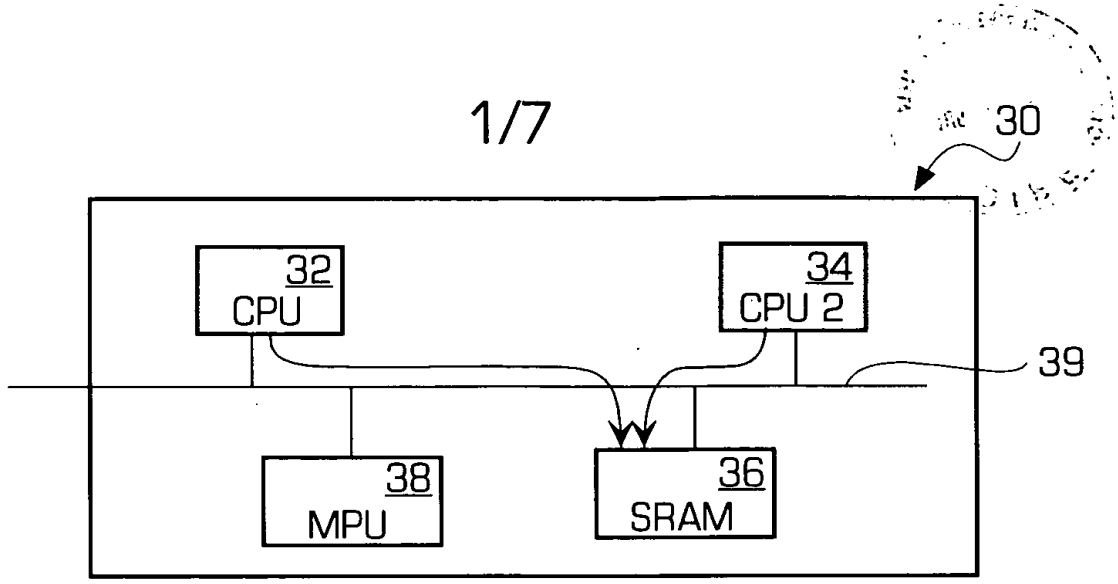

FIG. 1

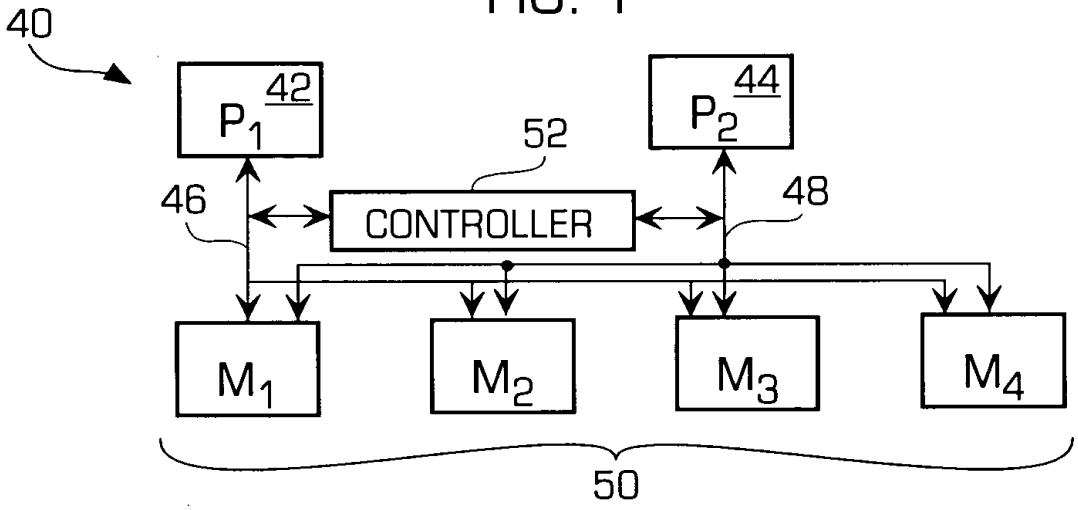

FIG. 2

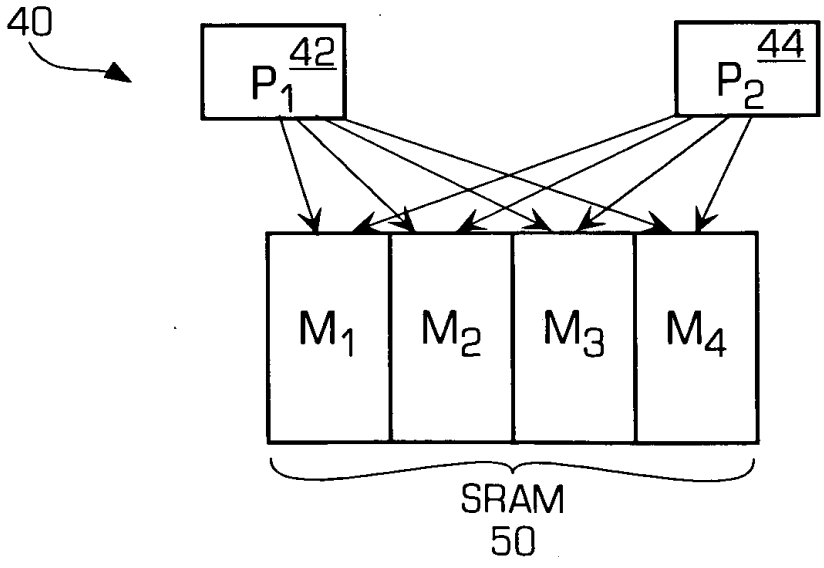

FIG. 3

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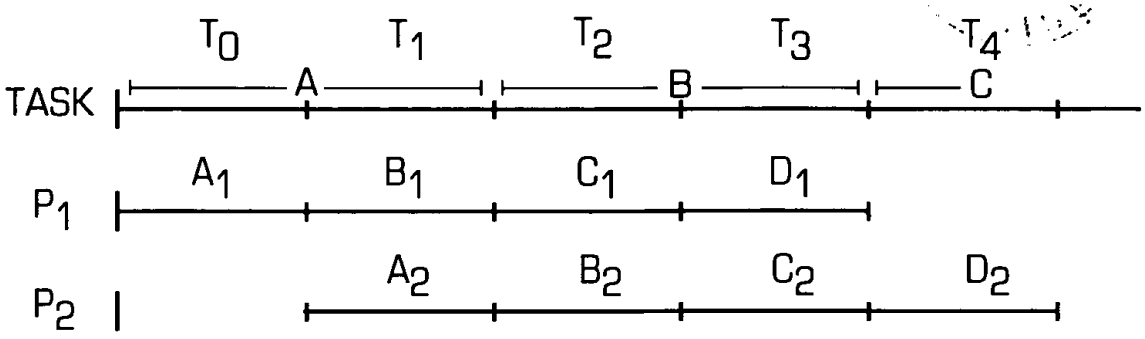

FIG. 4

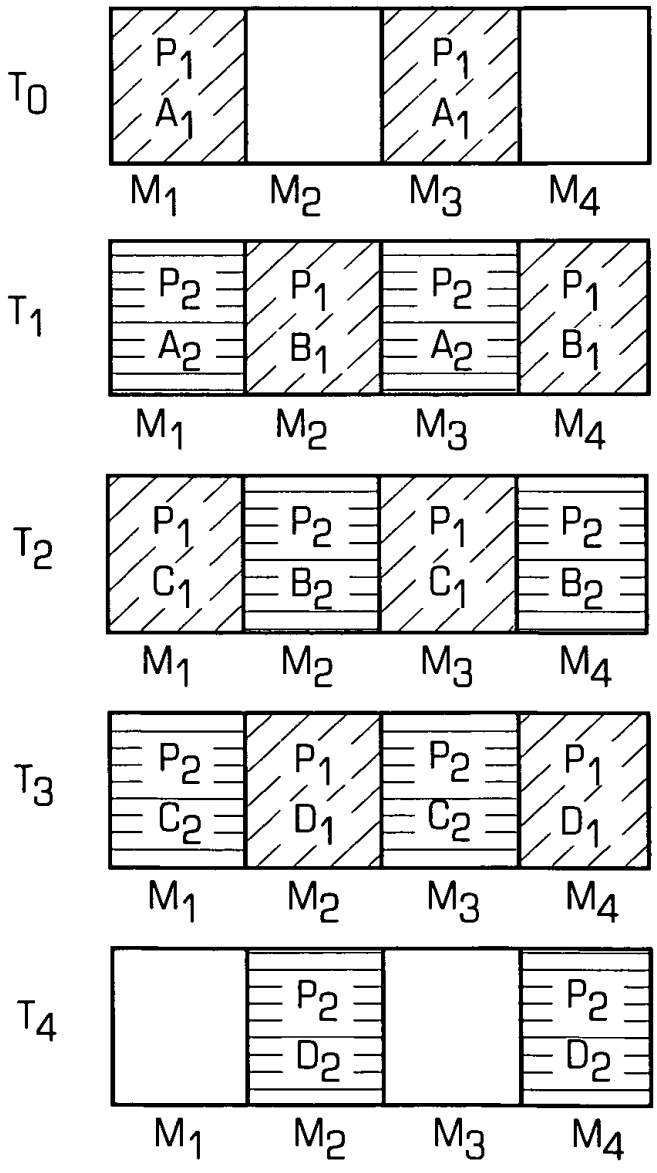

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

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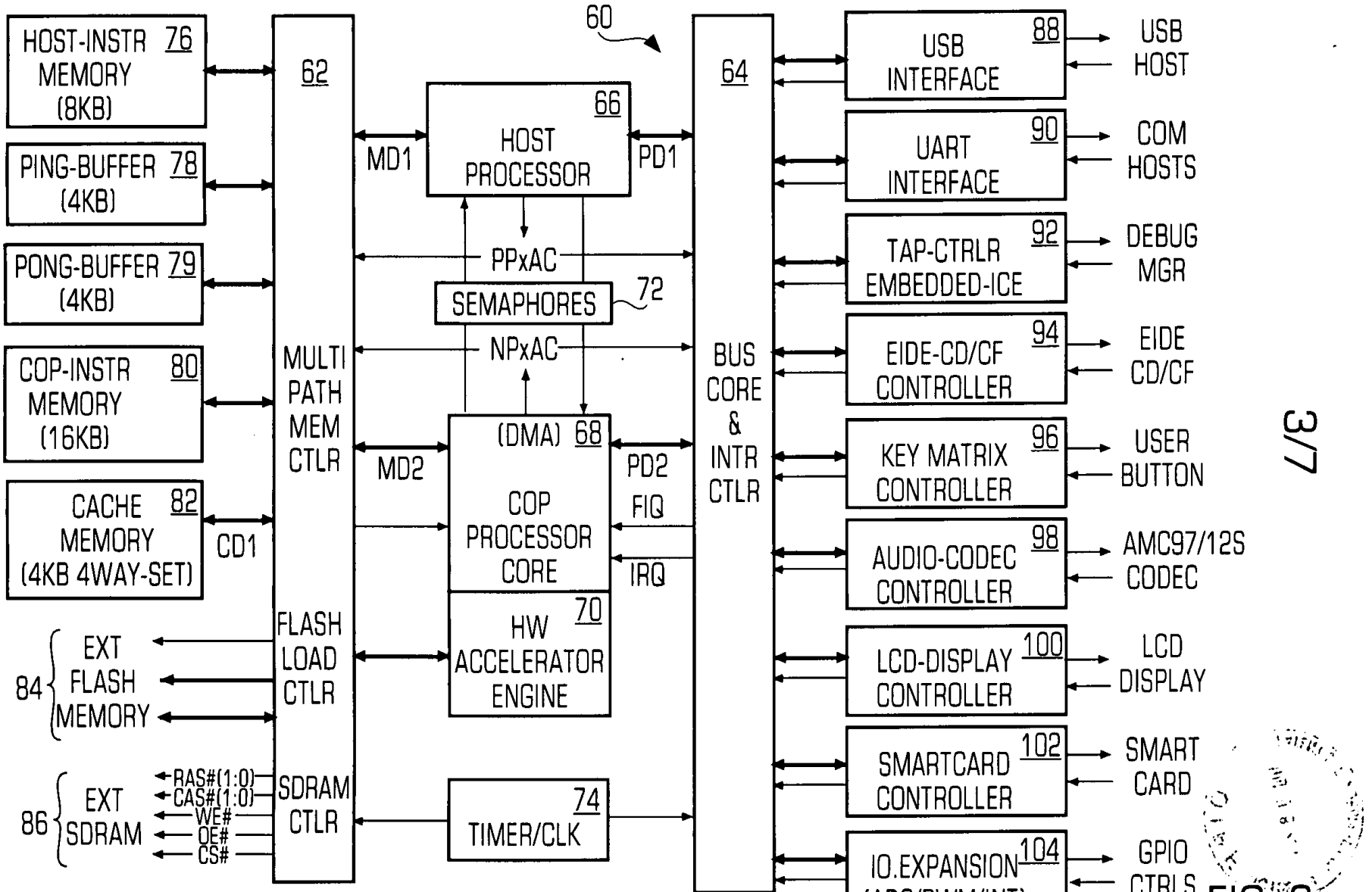

FUNCTIONAL BLOCK DIAGRAM OF SDMI-SOC

FIG. 6

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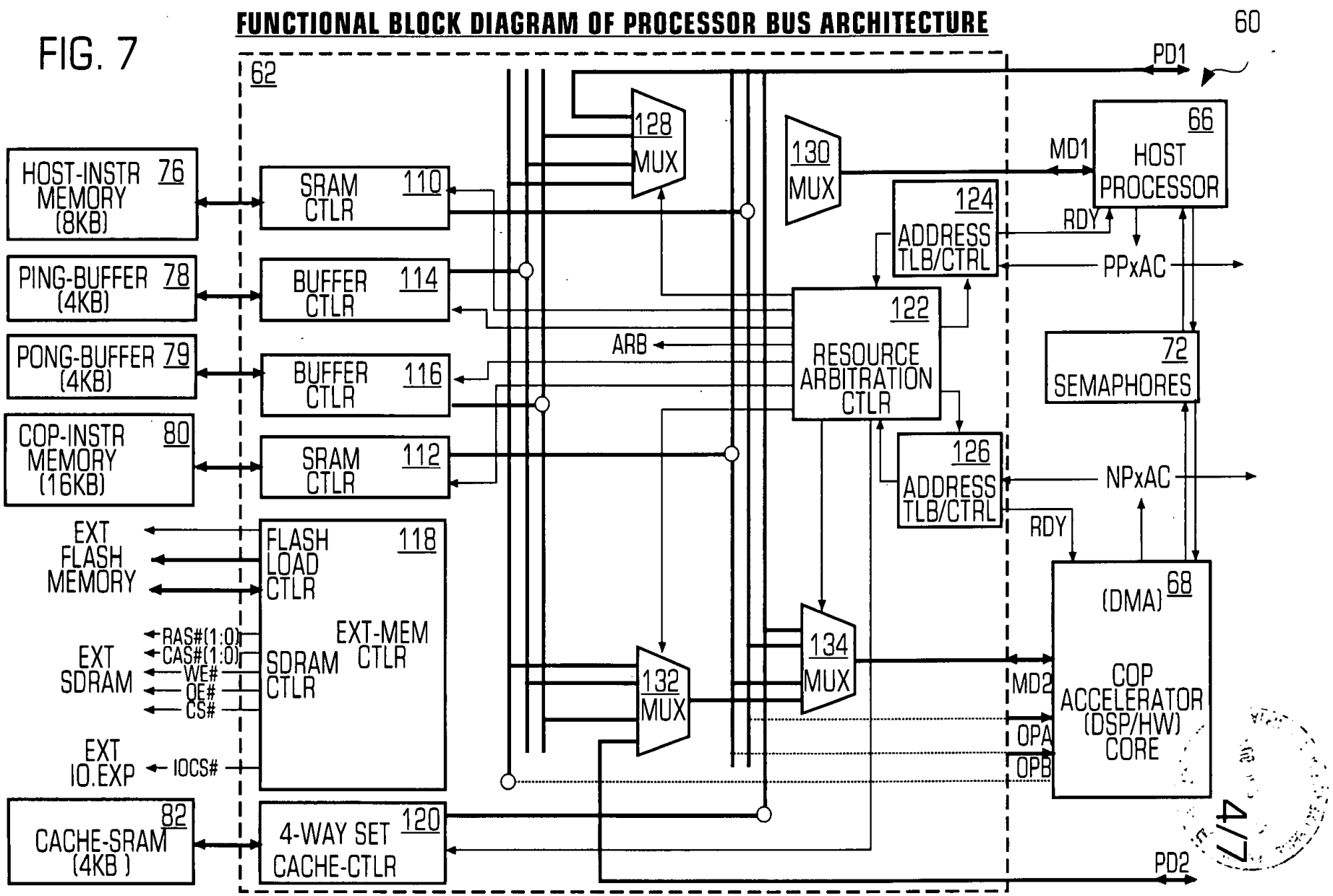
FIG. 7



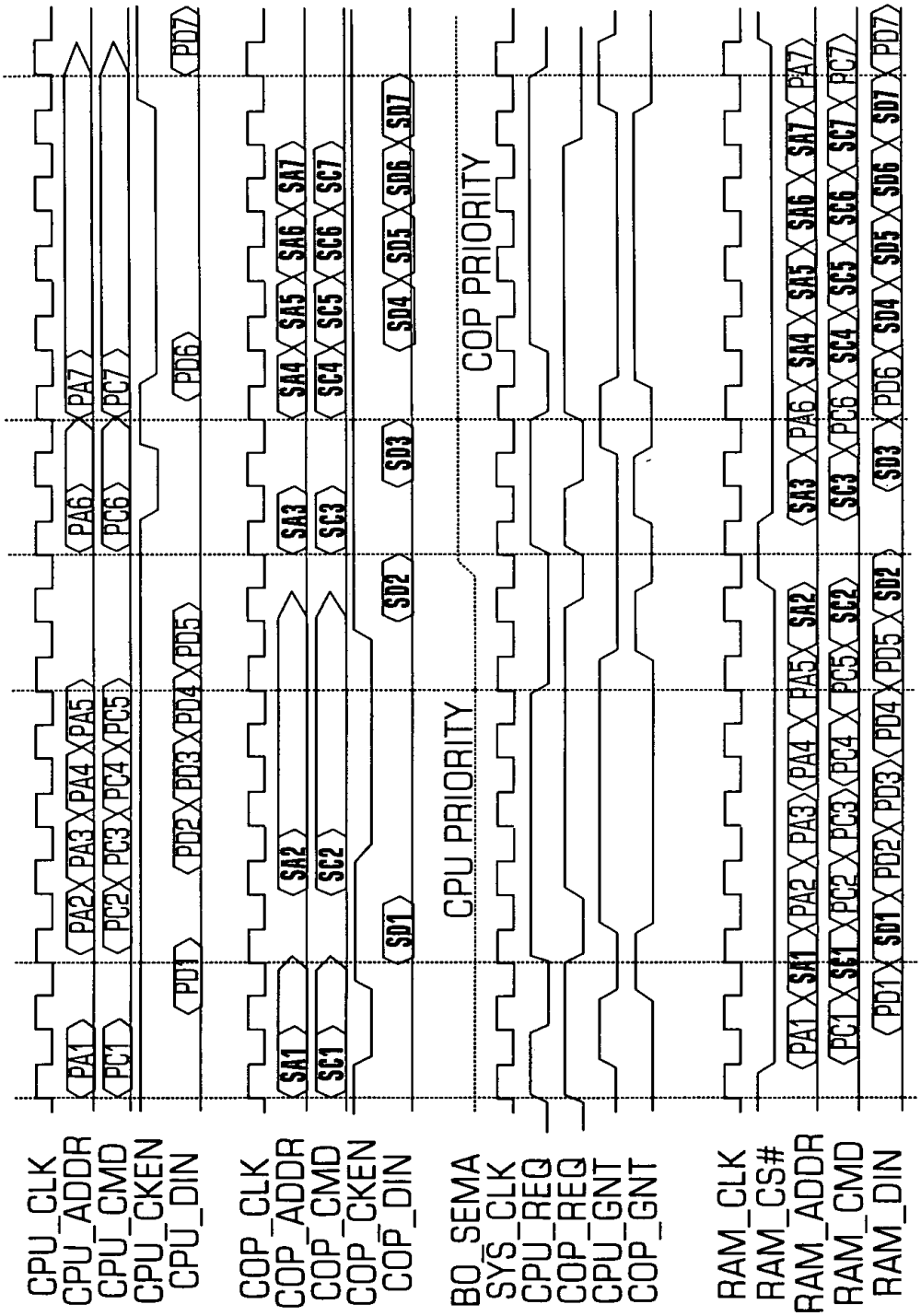

CPU_CLK
CPU_ADDR
CPU_CMD
CPU_CKEN
CPU_DIN
COP_CLK
COP_ADDR
COP_CMD
COP_CKEN
COP_DIN
BO_SEMA
SYS_CLK
CPU_REQ
COP_REQ
CPU_GNT
COP_GNT
RAM_CLK
RAM_CS#
RAM_ADDR
RAM_CMD
RAM_DIN
CPU PRIORITY
COP PRIORITY

FIG. 8

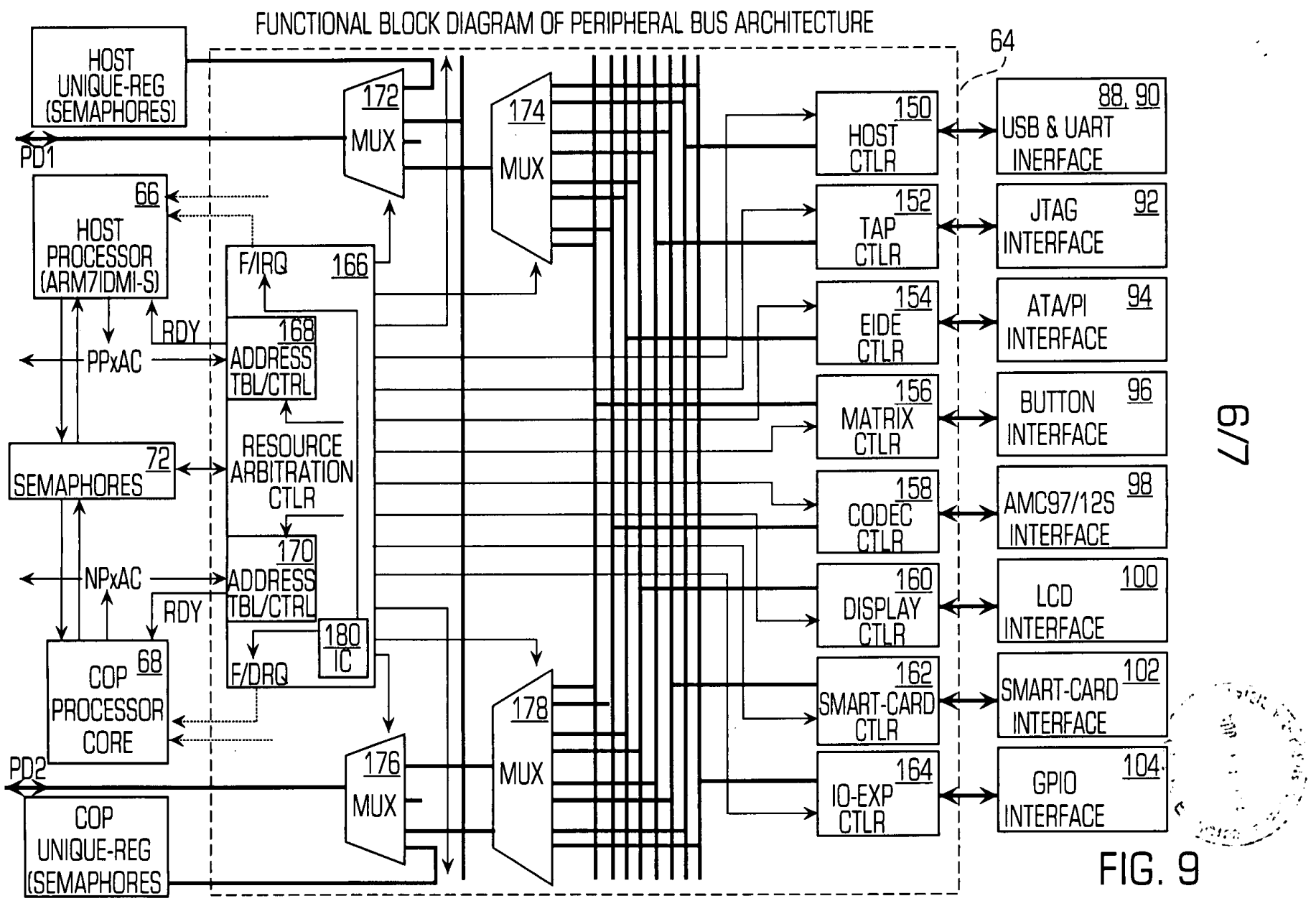

FUNCTIONAL BLOCK DIAGRAM OF PERIPHERAL BUS ARCHITECTURE
HOST UNIQUE-REG (SEMAPHORES)
PD1
66
HOST PROCESSOR (ARM7IDMI-S)
RDY
PPxAC
NPxAC
RDY
72
SEMAPHORES
COP 68
PROCESSOR CORE
PD2
COP UNIQUE-REG (SEMAPHORES
172
MUX
174
MUX
176
MUX
178
MUX
F/IRQ 166
168
ADDRESS TBL/CTRL
RESOURCE ARBITRATION CTLR
170
ADDRESS TBL/CTRL
180
TC
F/DRQ
64
150
HOST CTLR
152
TAP CTLR
154
EIDE CTLR
156
MATRIX CTLR
158
CODEC CTLR
160
DISPLAY CTLR
162
SMART-CARD CTLR
164
IO-EXP CTLR
88, 90
USB & UART INERFACE
92
JTAG INTERFACE
94
ATA/PI INTERFACE
96
BUTTON INTERFACE
98
AMC97/12S INTERFACE
100
LCD INTERFACE
102
SMART-CARD INTERFACE
104
GPIO INTERFACE

FIG. 9

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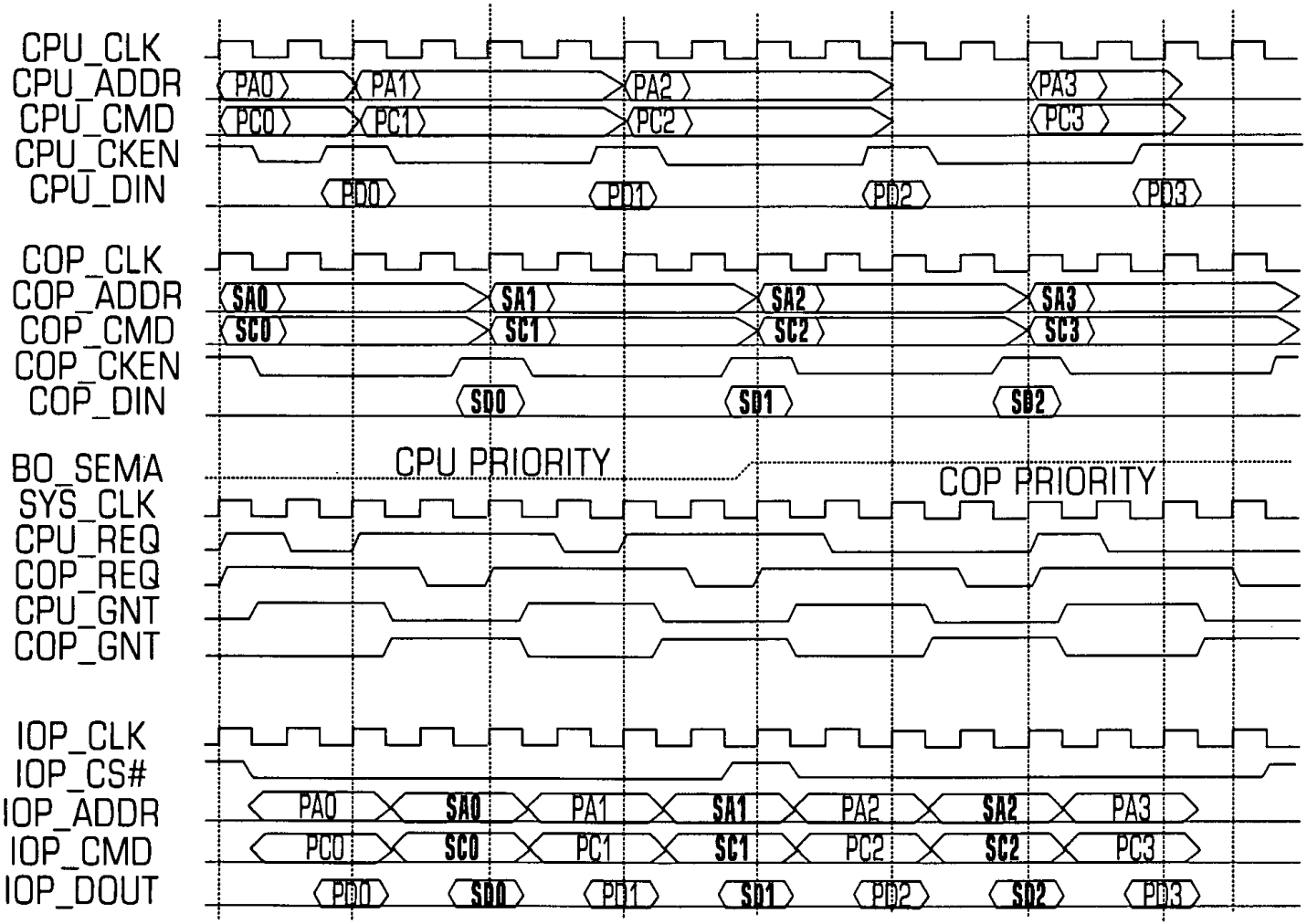

FIG. 10